

# RF LDMOS Wideband Integrated Power Amplifiers

The MW7IC930N wideband integrated circuit is designed with on-chip matching that makes it usable from 728 to 960 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulation.

## Driver Application — 900 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 106$  mA,  $I_{DQ2} = 285$  mA,  $P_{out} = 3.2$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency (1)	G <sub>ps</sub> (dB)	PAE (%)	ACPR (dBc)
920 MHz	36.6	16.1	-48.0
940 MHz	36.8	16.7	-48.7
960 MHz	36.6	17.3	-48.6

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 48 Watts CW Output Power (3 dB Input Overdrive from Rated P<sub>out</sub>)
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 30 Watts CW P<sub>out</sub>.
- Typical P<sub>out</sub> @ 1 dB Compression Point ≈ 31 Watts CW,  $I_{DQ1} = 40$  mA,  $I_{DQ2} = 340$  mA

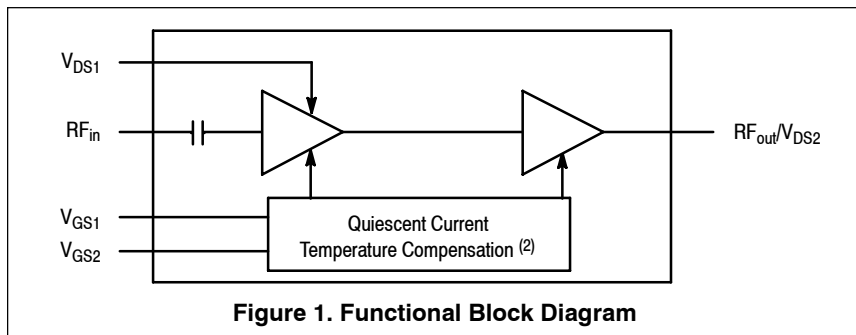
## Driver Application — 700 MHz

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 106$  mA,  $I_{DQ2} = 285$  mA,  $P_{out} = 3.2$  Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G <sub>ps</sub> (dB)	PAE (%)	ACPR (dBc)
728 MHz	36.4	16.1	-47.7
748 MHz	36.4	16.1	-47.8
768 MHz	36.4	16.0	-47.9

## Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/ Disable Function (2)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.



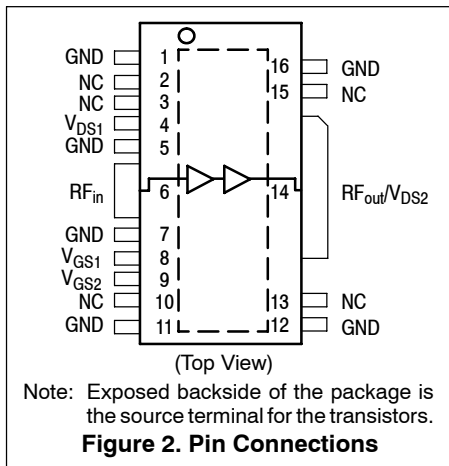
**MW7IC930NR1**  
**MW7IC930GNR1**  
**MW7IC930NBR1**

**728-768 MHz, 920-960 MHz,**  
**3.2 W AVG., 28 V**  
**SINGLE W-CDMA**  
**RF LDMOS WIDEBAND**  
**INTEGRATED POWER AMPLIFIERS**

**CASE 1886-01**  
**TO-270 WB-16**  
**PLASTIC**  
**MW7IC930NR1**

**CASE 1887-01**  
**TO-270 WB-16 GULL**  
**PLASTIC**  
**MW7IC930GNR1**

**CASE 1329-09**  
**TO-272 WB-16**  
**PLASTIC**  
**MW7IC930NBR1**



1. 900 MHz Driver Frequency Band table data collected in the 900 MHz application test fixture. See Fig. 7.  
 2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	20	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case (Case Temperature 80°C, 3.2 W CW)	$R_{\theta JC}$	Stage 1, 28 Vdc, $I_{DQ1} = 106$ mA	°C/W
		Stage 2, 28 Vdc, $I_{DQ2} = 285$ mA	
(Case Temperature 80°C, 30 W CW)		Stage 1, 28 Vdc, $I_{DQ1} = 40$ mA	
		Stage 2, 28 Vdc, $I_{DQ2} = 340$ mA	

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	II (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Stage 1 — Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 1 — On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 14$ $\mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1} = 106$ mA)	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage (4) ( $V_{DD} = 28$ Vdc, $I_{DQ1} = 106$ mA, Measured in Functional Test)	$V_{GG(Q)}$	6.9	9.4	11.9	Vdc

- Continuous use at maximum temperature will affect MTTF.
- MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
- Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
- $V_{GG} = 3.3 \times V_{GS(Q)}$ . Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 — Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{A dc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{A dc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{A dc}$

**Stage 2 — On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 74\ \mu\text{A dc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2} = 285\text{ mA}$ )	$V_{GS(Q)}$	—	2.6	—	Vdc
Fixture Gate Quiescent Voltage (1) ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2} = 285\text{ mA}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.2	5.9	7.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 740\text{ mA}$ )	$V_{DS(on)}$	0.1	0.3	0.8	Vdc

**Functional Tests** (2,3) (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 106\text{ mA}$ ,  $I_{DQ2} = 285\text{ mA}$ ,  $P_{out} = 3.2\text{ W Avg.}$ ,  $f = 940\text{ MHz}$ , Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carrier, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	33	35.9	38	dB
Power Added Efficiency	PAE	14	16.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-49.5	-46	dBc
Input Return Loss	IRL	—	-18.7	-9	dB

**Typical Broadband Performance — 900 MHz** (In Freescale 900 MHz Application Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 106\text{ mA}$ ,  $I_{DQ2} = 285\text{ mA}$ ,  $P_{out} = 3.2\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)	IRL (dB)
920 MHz	36.6	16.1	-48.0	-19.9
940 MHz	36.8	16.7	-48.7	-20.8
960 MHz	36.6	17.3	-48.6	-19.7

- $V_{GG} = 2.25 \times V_{GS(Q)}$ . Parameter measured on Freescale Test Fixture, due to resistive divider network on the board. Refer to Test Circuit schematic.
- Part internally matched both on input and output.
- Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

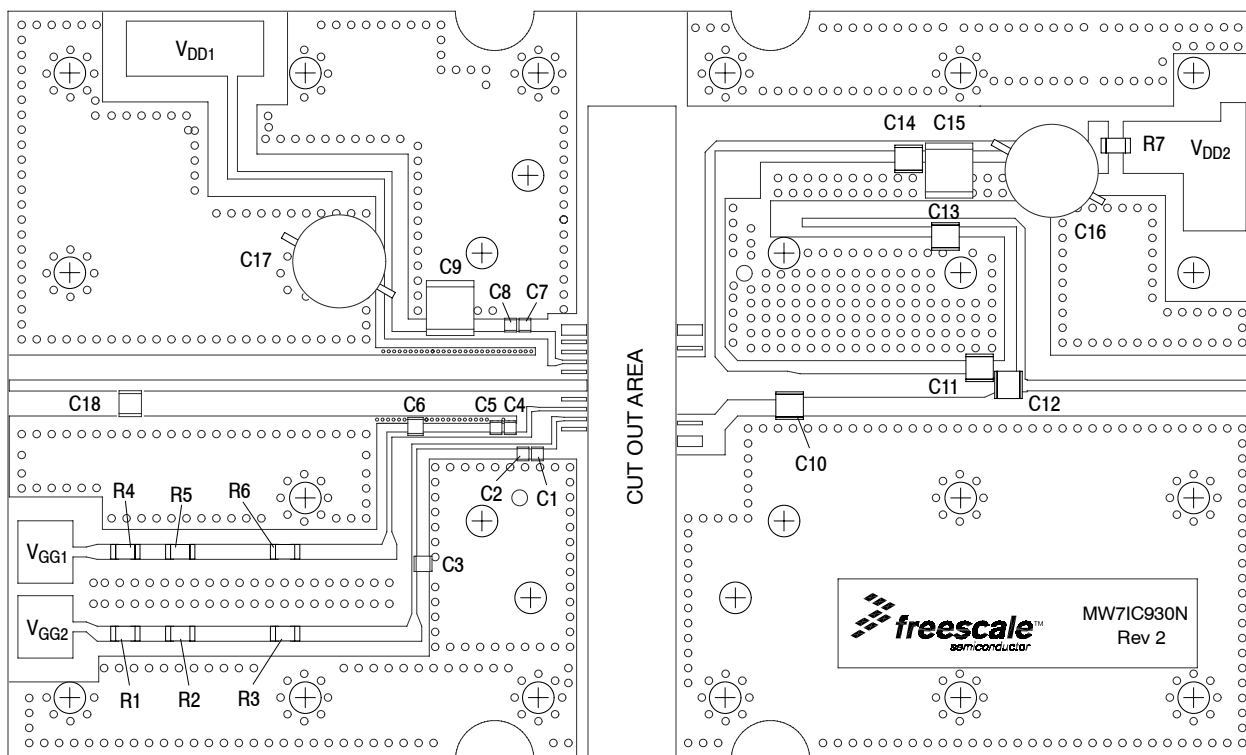
**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performance — 900 MHz</b> (In Freescale 900 MHz Application Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1} = 106\text{ mA}$ , $I_{DQ2} = 285\text{ mA}$ , 920-960 MHz Bandwidth					
$V_{DD} = 28\text{ Vdc}$ , $I_{DQ1} = 40\text{ mA}$ , $I_{DQ2} = 340\text{ mA}$ $P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	31	—	W
IMD Symmetry @ 25 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD <sub>sym</sub>	—	45	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	80	—	MHz
Quiescent Current Accuracy over Temperature <sup>(1)</sup> with 3 k $\Omega$ Gate Feed Resistors (-30 to 85°C)	$\Delta I_{QT}$	—	0.02	—	%
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 3.2\text{ W Avg.}$	$G_F$	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.036	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1\text{dB}$	—	0.01	—	dBm/°C

**Typical W-CDMA Broadband Performance — 700 MHz** (In Freescale 700 MHz Application Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 106\text{ mA}$ ,  $I_{DQ2} = 285\text{ mA}$ ,  $P_{out} = 3.2\text{ W Avg.}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Frequency	$G_{ps}$ (dB)	PAE (%)	ACPR (dBc)	IRL (dB)
728 MHz	36.4	16.1	-47.7	-17.9
748 MHz	36.4	16.1	-47.8	-20.7
768 MHz	36.4	16.0	-47.9	-21.8

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

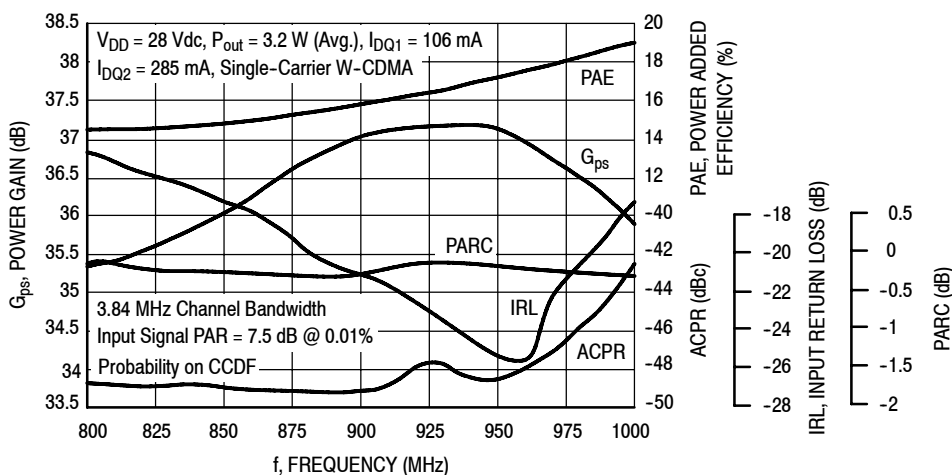


**Figure 3. MW7IC930NR1(GNR1)(NBR1) Test Circuit Component Layout — 900 MHz**

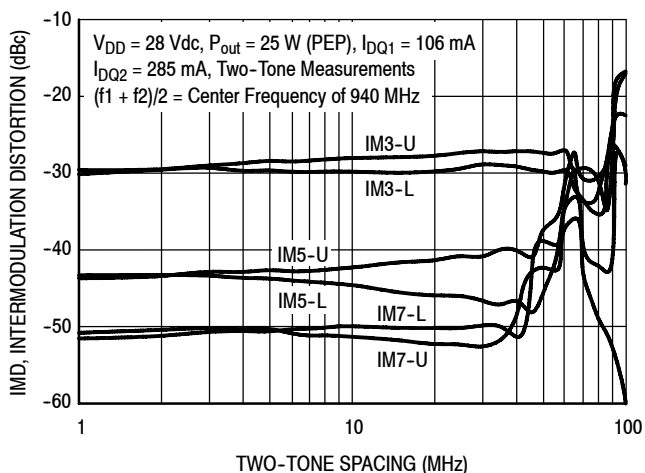
**Table 6. MW7IC930NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 900 MHz**

Part	Description	Part Number	Manufacturer
C1, C4, C7	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C2, C5, C8	10 nF, 50 V Chip Capacitors	C0603C103J5RAC-TU	Kemet
C3, C6	1 $\mu$ F, 50 V Chip Capacitors	GRM21BR71H105KA12L	Murata
C9, C15	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C10	16 pF Chip Capacitor	ATC100B160JT500XT	ATC
C11	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C12	7.5 pF Chip Capacitor	ATC100B7R5CT500XT	ATC
C13, C14	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C16, C17	100 $\mu$ F, 50 V Electrolytic Capacitors	MCGPR35V337M10X16-RH	Multicomp
C18	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2, R3, R4, R5, R6	1000 $\Omega$ , 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R7	0 $\Omega$ , 3A Chip Resistor	CRCW12060000Z0EA	Vishay
PCB	0.020", $\epsilon_r = 3.5$	RF-35	Taconic

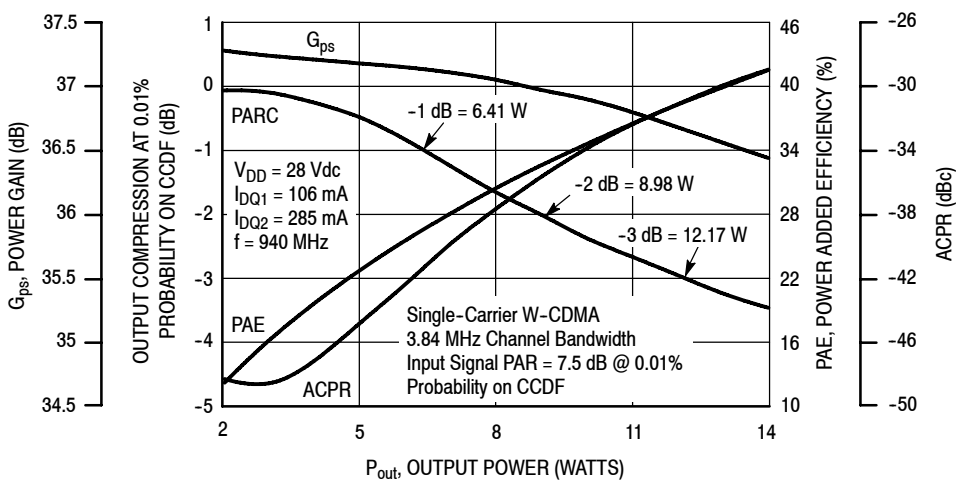
### TYPICAL CHARACTERISTICS — 900 MHz



**Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 3.2$  Watts Avg.**

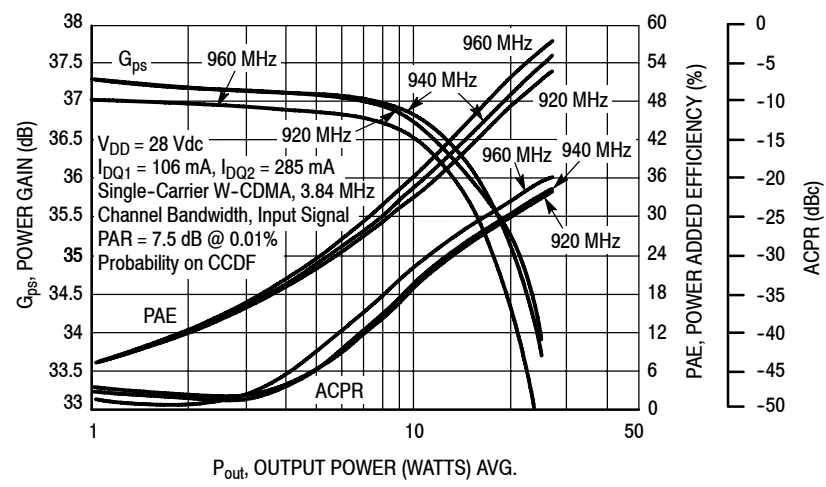


**Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing**

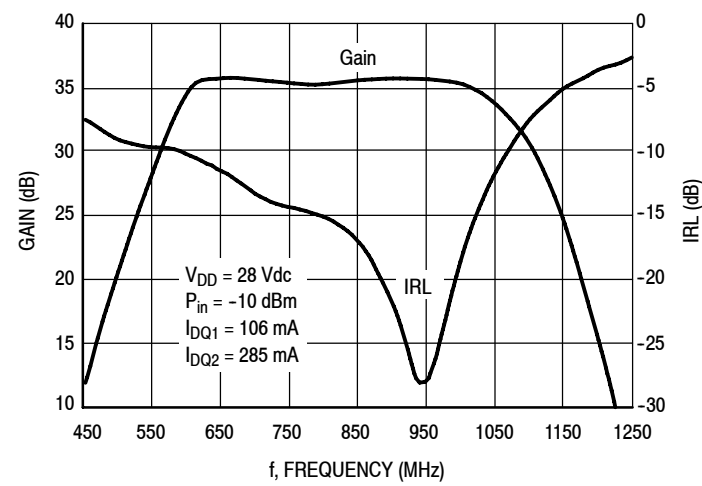


**Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power**

### TYPICAL CHARACTERISTICS — 900 MHz

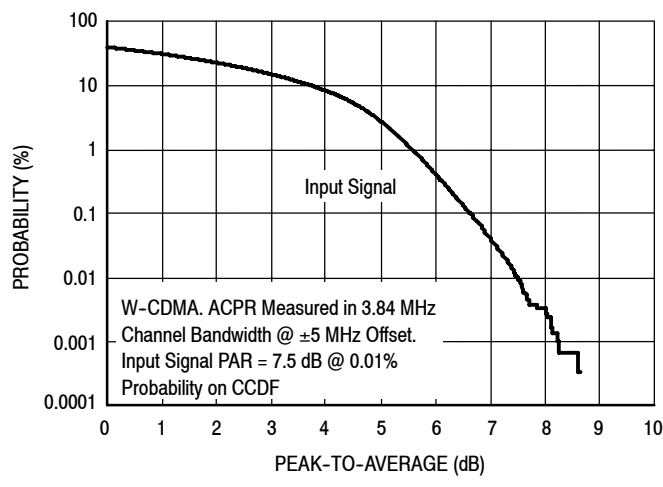


**Figure 7. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**

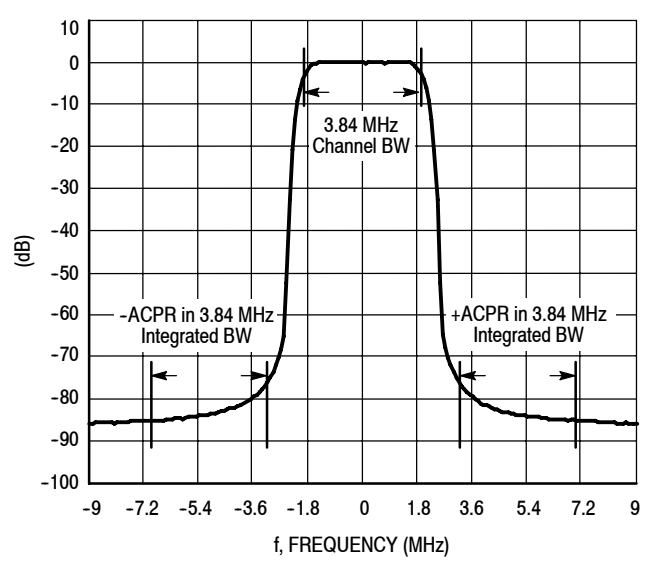


**Figure 8. Broadband Frequency Response**

### W-CDMA TEST SIGNAL



**Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal**



**Figure 10. Single-Carrier W-CDMA Spectrum**

MW7IC930NR1 MW7IC930GMR1 MW7IC930NBR1

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 106 \text{ mA}$ ,  $I_{DQ2} = 285 \text{ mA}$ ,  $P_{out} = 3.2 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
820	$37.95 + j2.31$	$4.70 + j0.98$
840	$39.95 + j2.72$	$4.29 + j1.23$
860	$42.70 + j1.02$	$3.93 + j1.67$
880	$44.40 - j1.38$	$3.63 + j2.15$
900	$46.25 - j4.92$	$3.41 + j2.61$
920	$45.70 - j8.41$	$3.14 + j3.05$
940	$45.46 - j11.47$	$2.94 + j3.48$
960	$45.07 - j15.19$	$2.85 + j3.90$
980	$43.49 - j18.03$	$2.69 + j4.32$

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

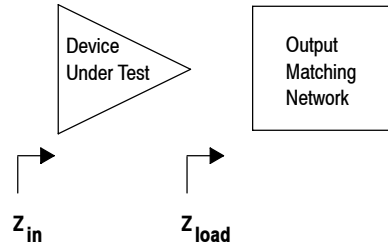
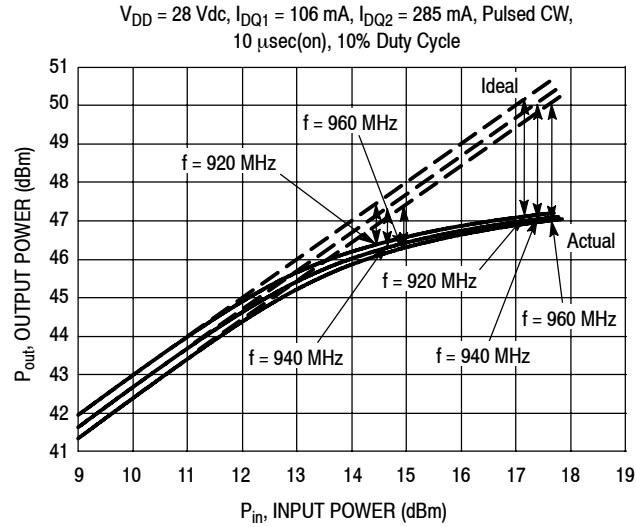


Figure 11. Series Equivalent Input and Load Impedance — 900 MHz



## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS — 900 MHz



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
920	43	46.3	51	47.1
940	42	46.3	50	47
960	42	46.3	50	47

Test Impedances per Compression Level

f (MHz)		$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
920	P1dB	55.82 + j15.71	4.54 + j1.15
940	P1dB	52.56 + j20.20	4.38 + j1.21
960	P1dB	49.18 + j25.00	5.04 + j1.15

**Figure 12. Pulsed CW Output Power versus Input Power @ 28 V**

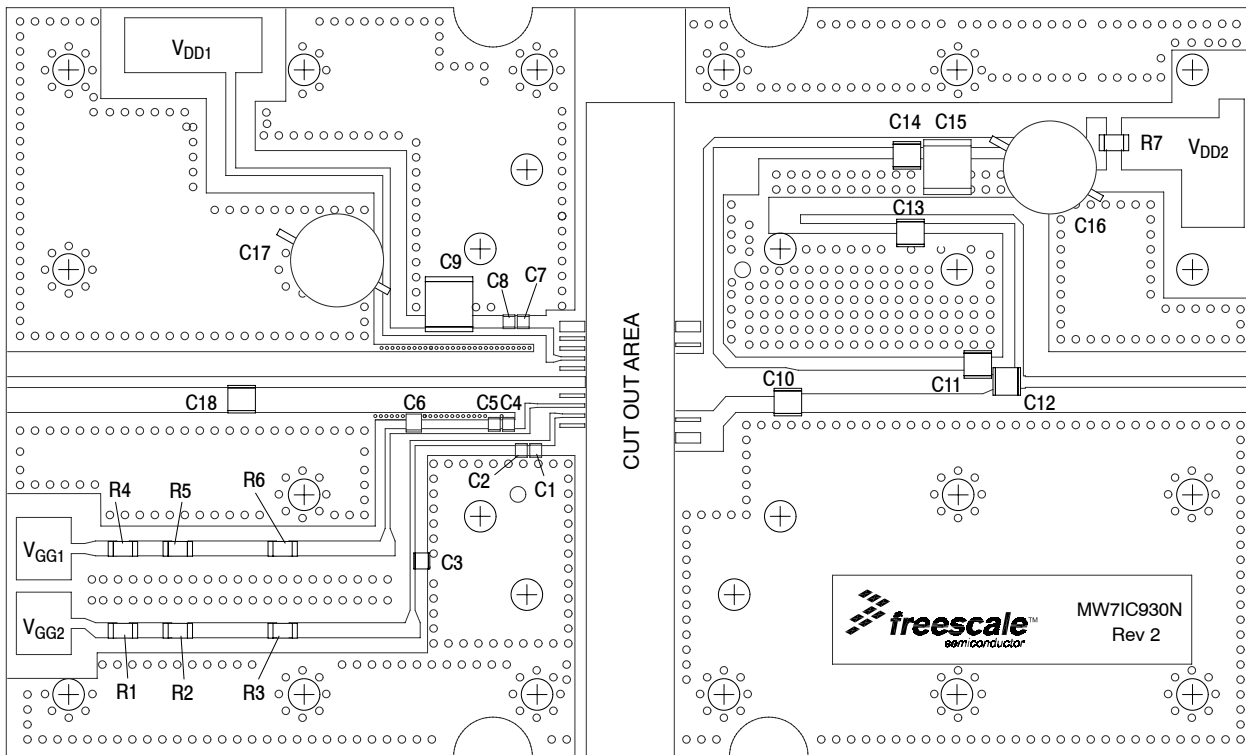
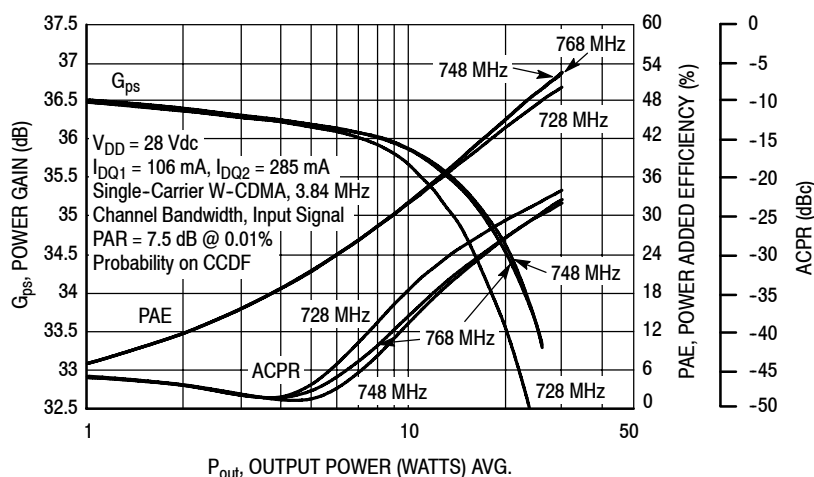


Figure 13. MW7IC930NR1(GNR1)(NBR1) Test Circuit Component Layout — 700 MHz

Table 7. MW7IC930NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 700 MHz

Part	Description	Part Number	Manufacturer
C1, C4, C7	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C2, C5, C8	10 nF, 50 V Chip Capacitors	C0603C103J5RAC	Kemet
C3, C6	1 $\mu$ F, 50 V Chip Capacitors	GRM21BR71H105KA12L	Murata
C9, C15	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C10	13 pF Chip Capacitor	ATC100B130JT500XT	ATC
C11	7.5 pF Chip Capacitor	ATC100B7R5CT500XT	ATC
C12	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C13, C14	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C16, C17	100 $\mu$ F, 50 V Electrolytic Capacitors	MCGPR35V337M10X16-RH	Multicomp
C18	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
R1, R2, R3, R4, R5, R6	1000 $\Omega$ , 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
R7	0 $\Omega$ , 3A Chip Resistor	CRCW12060000Z0EA	Vishay
PCB	0.020", $\epsilon_r = 3.5$	RF-35	Taconic

### TYPICAL CHARACTERISTICS — 700 MHz



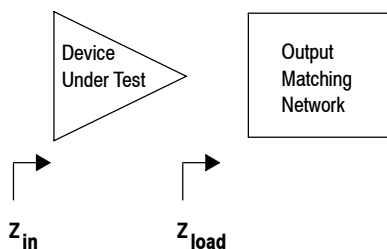
**Figure 14. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power — 700 MHz**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 106 \text{ mA}$ ,  $I_{DQ2} = 285 \text{ mA}$ ,  $P_{out} = 3.2 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
710	25.21 - j1.21	8.57 + j2.52
720	33.76 + j5.36	8.52 + j2.46
730	38.78 + j1.40	8.44 + j2.34
740	40.14 - j0.76	8.36 + j2.16
750	35.46 - j1.15	8.30 + j2.00
760	34.65 - j0.53	8.32 + j1.90
770	34.75 - j0.43	8.31 + j1.86
780	36.20 + j0.81	8.27 + j1.98
790	36.18 + j1.33	8.23 + j2.12

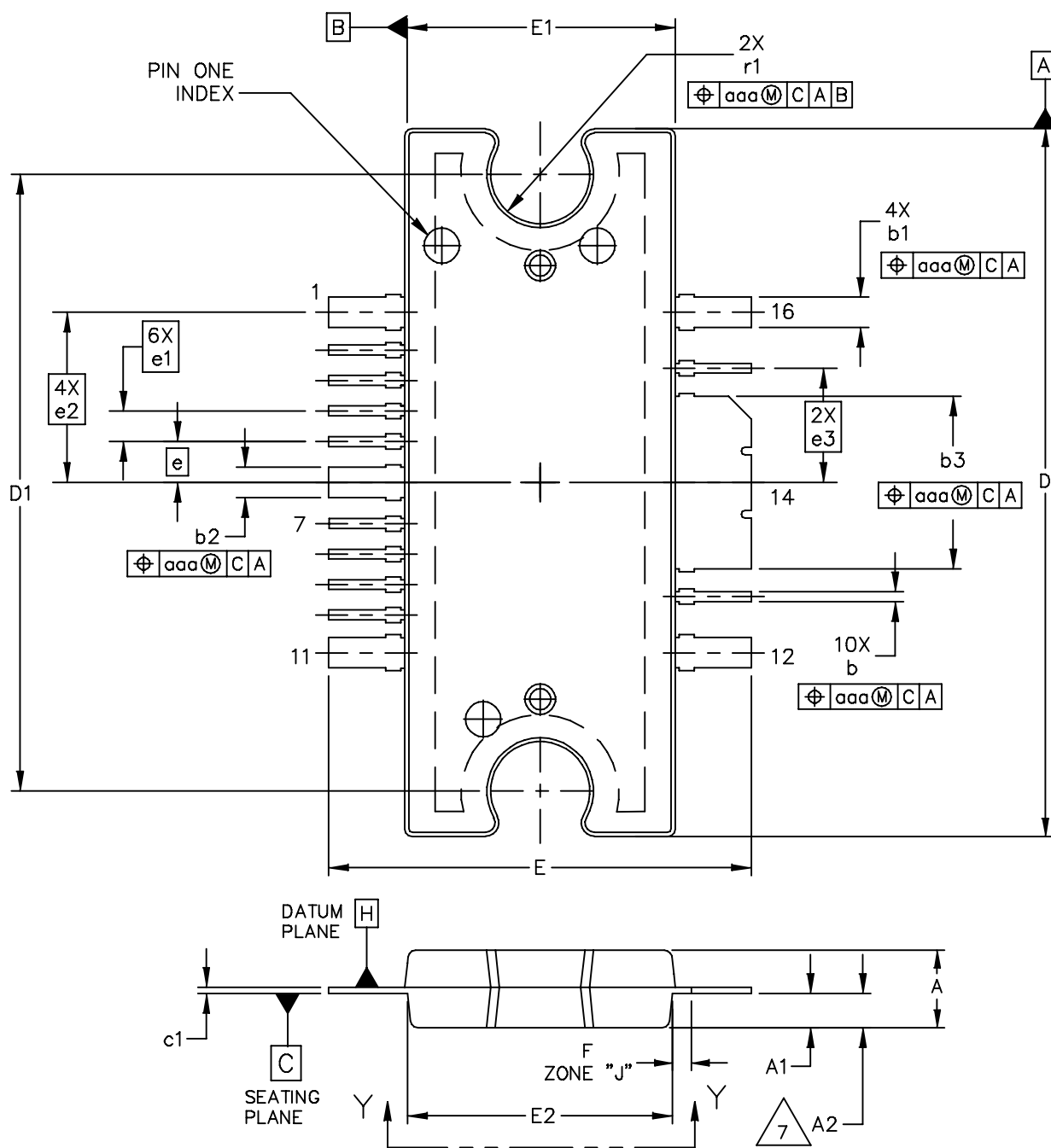
$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

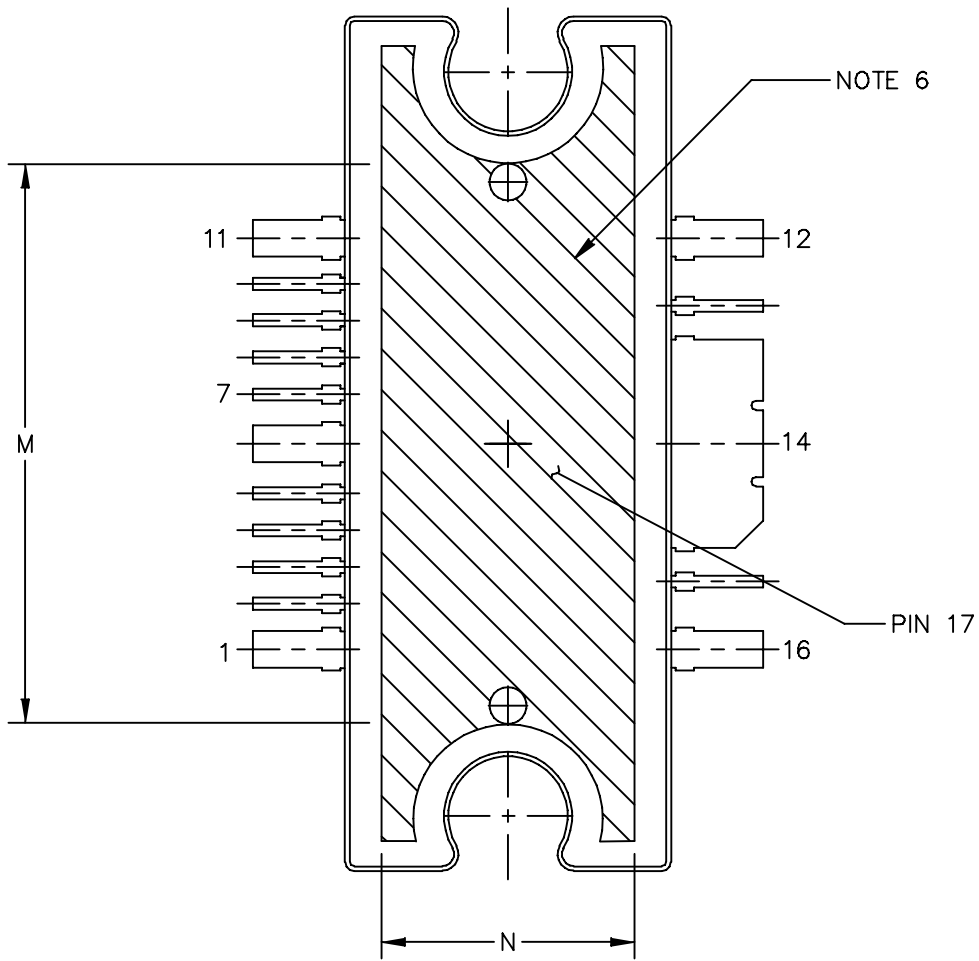


**Figure 15. Series Equivalent Input and Load Impedance — 700 MHz**

### PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A		REV: M
	CASE NUMBER: 1329-09		23 AUG 2007
	STANDARD: NON-JEDEC		



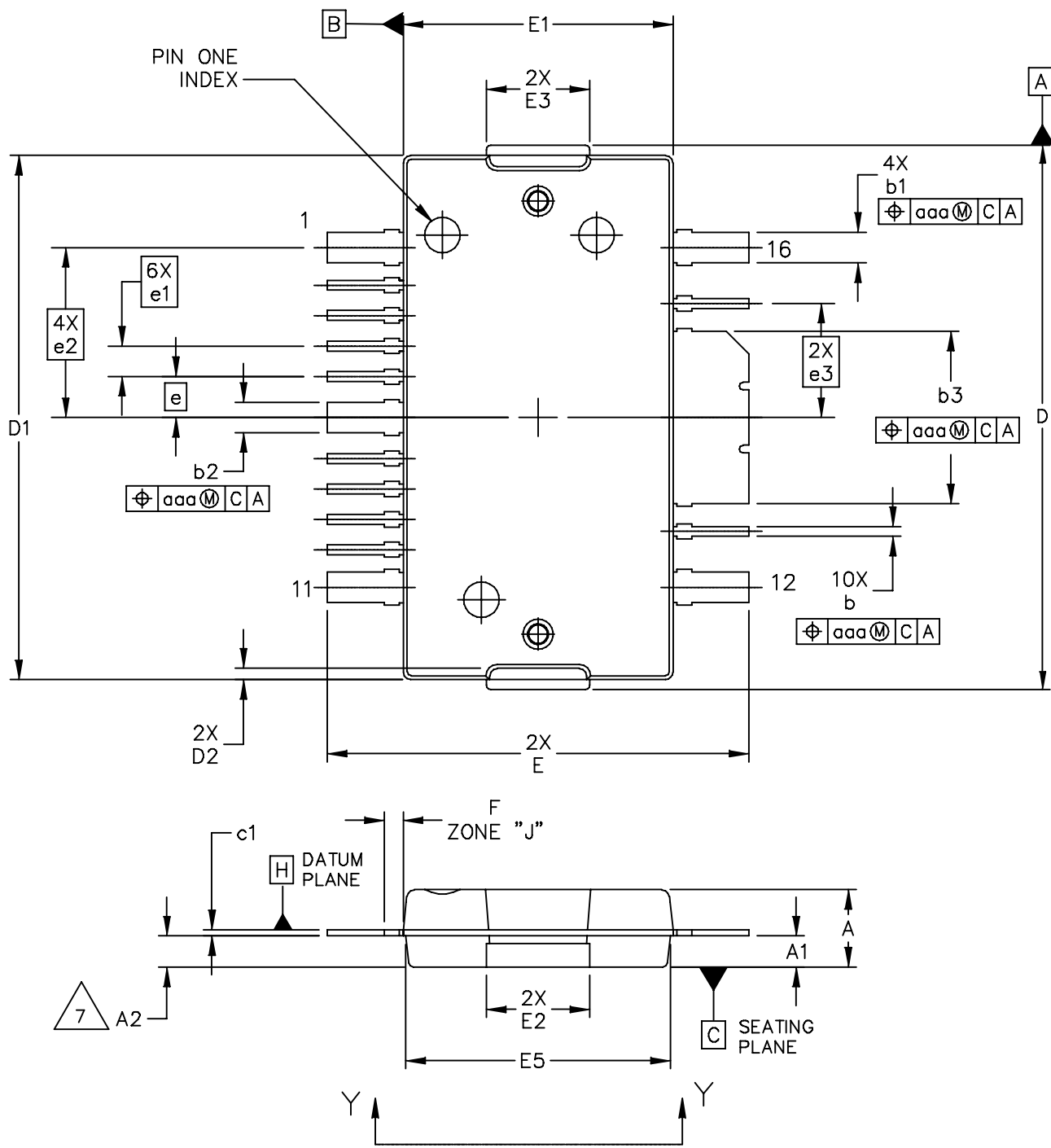
VIEW Y-Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A	REV: M	
	CASE NUMBER: 1329-09	23 AUG 2007	
	STANDARD: NON-JEDEC		

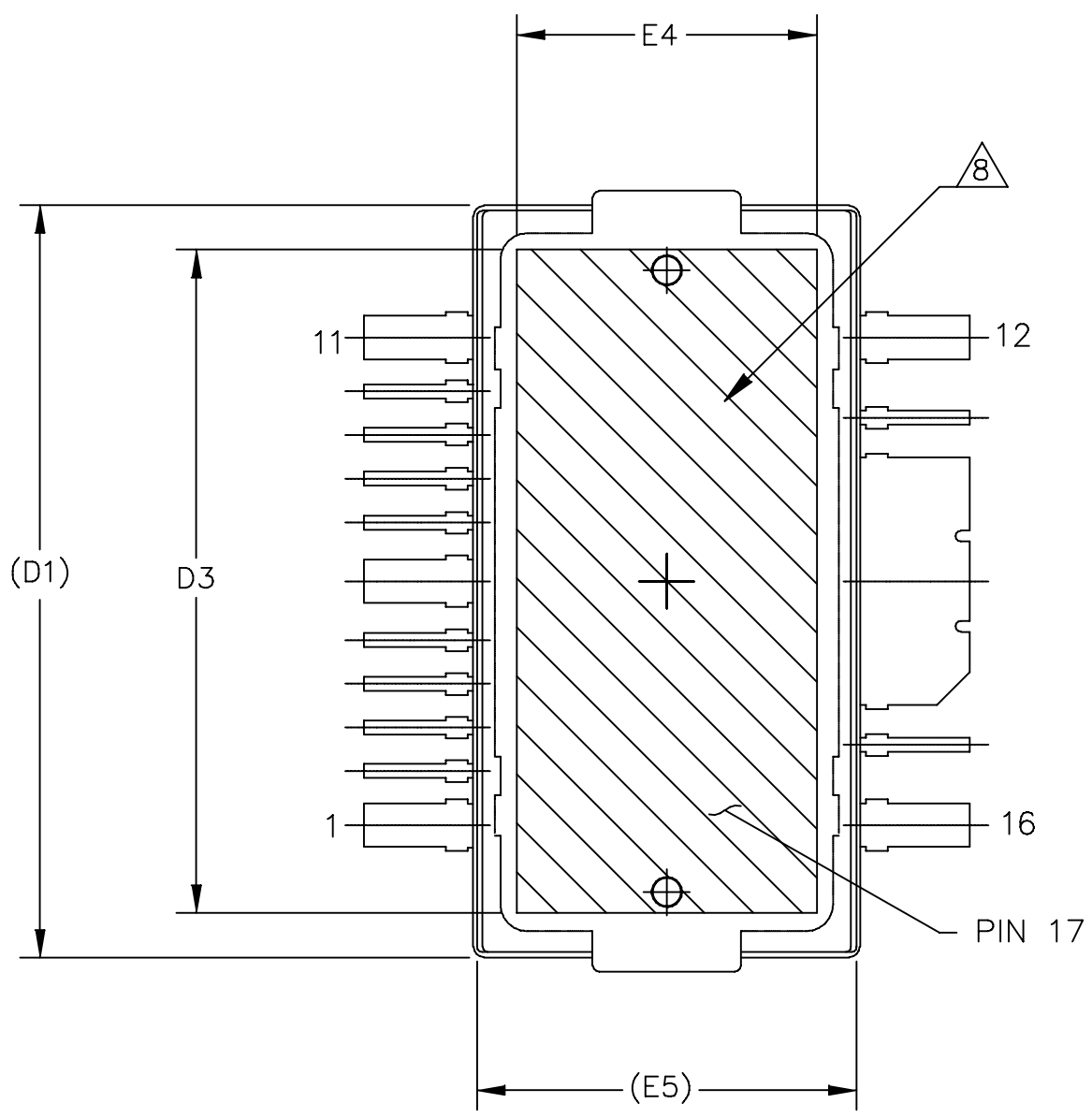
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	
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					CASE NUMBER: 1329-09			23 AUG 2007	
					STANDARD: NON-JEDEC				



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		CASE NUMBER: 1886-01		31 AUG 2007	
		STANDARD: NON-JEDEC			



VIEW Y-Y

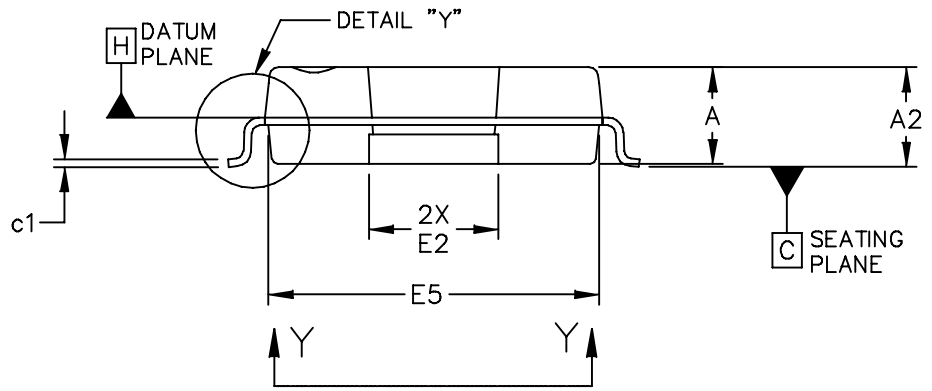
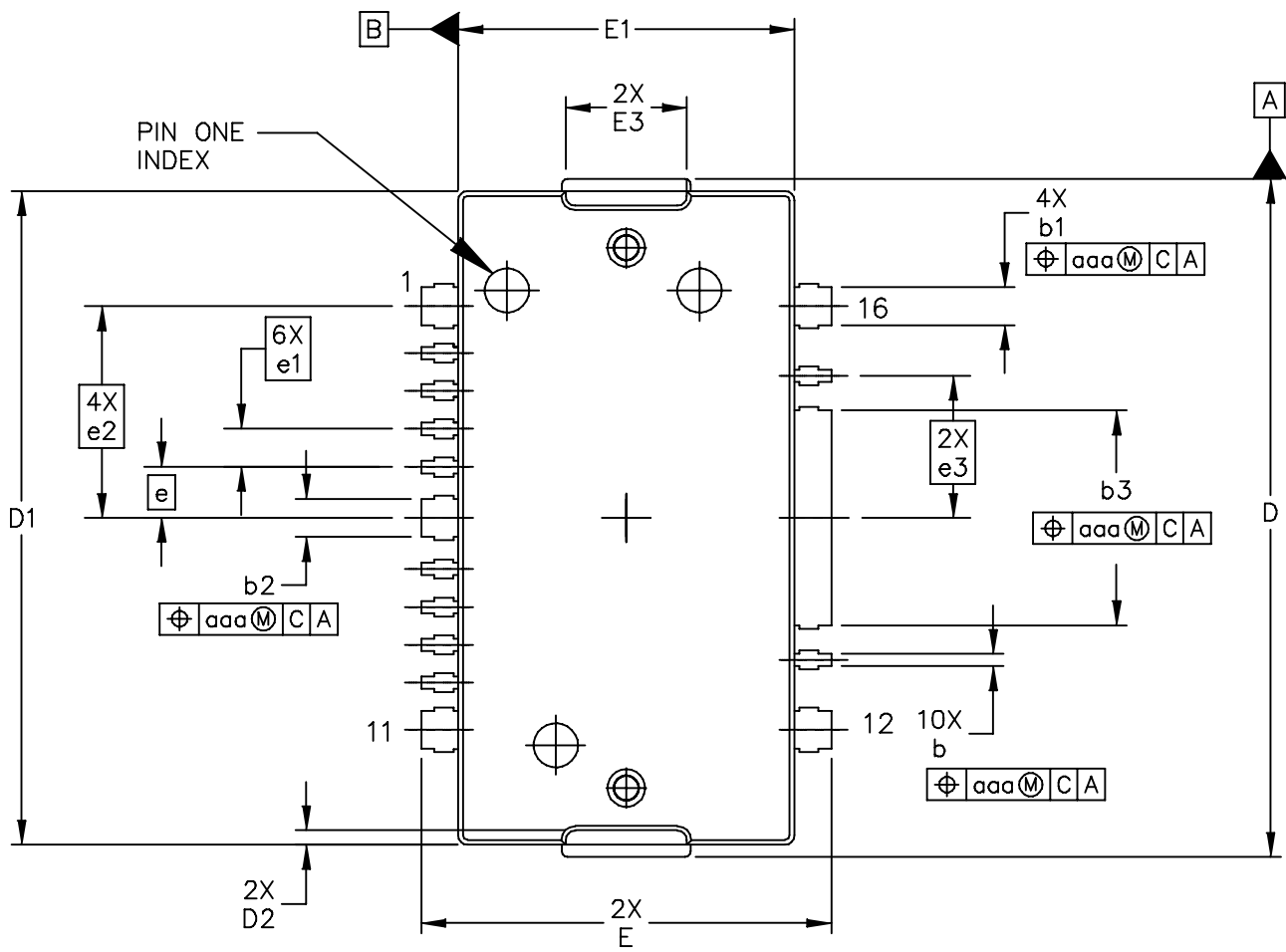
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TITLE: TO-270 WIDE BODY 16 LEAD	DOCUMENT NO: 98ASA10754D	REV: A	
	CASE NUMBER: 1886-01	31 AUG 2007	
	STANDARD: NON-JEDEC		



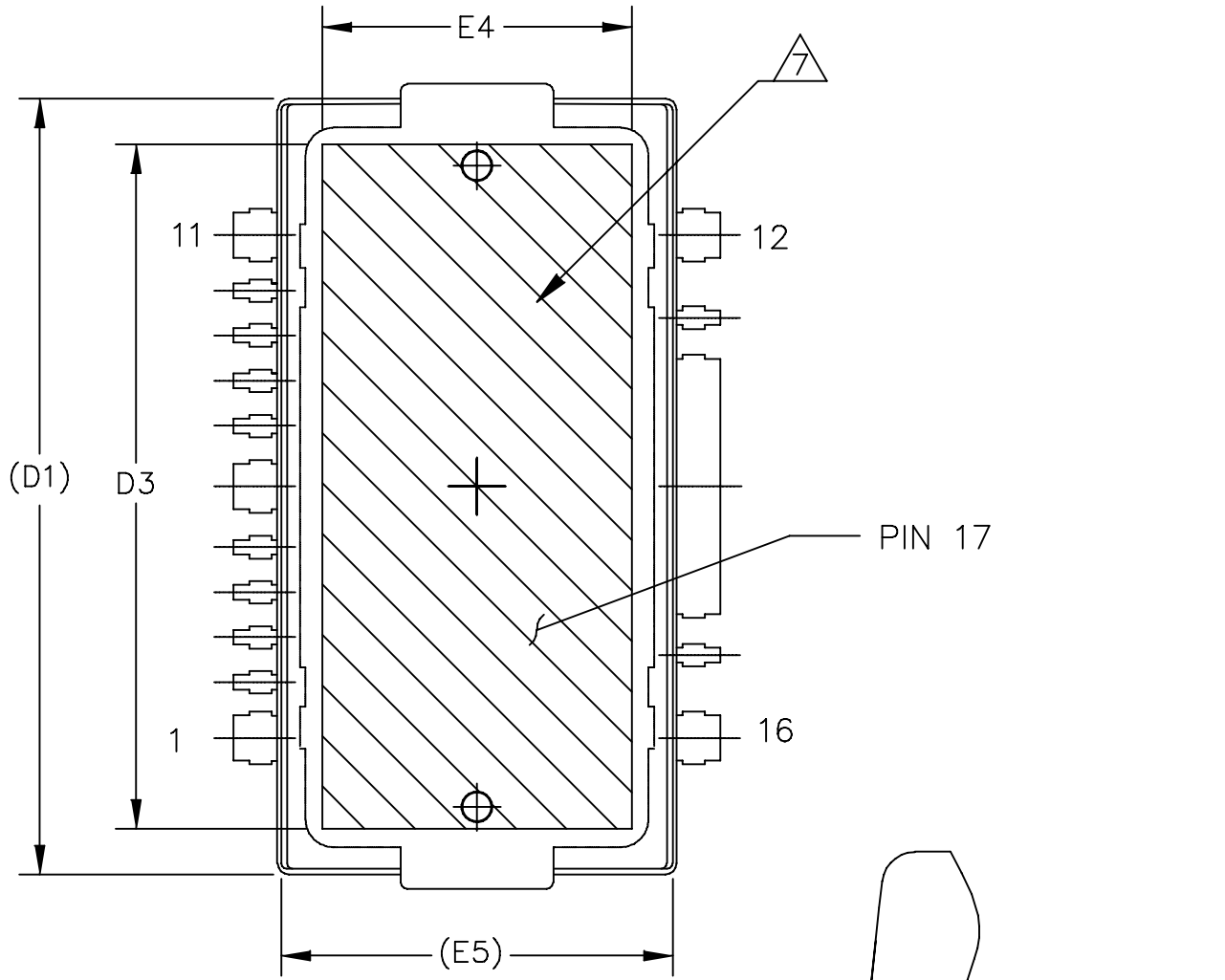
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

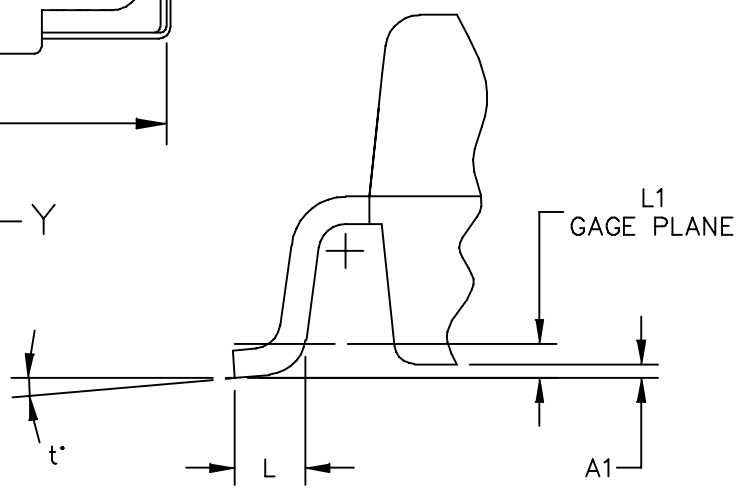
DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.011	.017	0.28	0.43
A2	.040	.042	1.02	1.07	b1	.037	.043	0.94	1.09
D	.712	.720	18.08	18.29	b2	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b3	.225	.231	5.72	5.87
D2	.011	.019	0.28	0.48	c1	.007	.011	.18	.28
D3	.600	---	15.24	---	e	.054 BSC		1.37 BSC	
E	.551	.559	14	14.2	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.224 BSC		5.69 BSC	
E2	.132	.140	3.35	3.56	e3	.150 BSC		3.81 BSC	
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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			CASE NUMBER: 1887-01		31 AUG 2007
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VIEW Y-Y



DETAIL "Y"

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	CASE NUMBER: 1887-01	31 AUG 2007	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.011	.017	0.28	0.43
D	.712	.720	18.08	18.29	b1	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b2	.037	.043	0.94	1.09
D2	.011	.019	0.28	0.48	b3	.225	.231	5.72	5.87
D3	.600	---	15.24	---	c1	.007	.011	0.18	0.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.132	.140	3.35	3.56	e2	.224 BSC		5.69 BSC	
E3	.124	.132	3.15	3.35	e3	.150 BSC		3.81 BSC	
E4	.270	---	6.86	---	t	2°	8°	2°	8°
E5	.346	.350	8.79	8.89	aaa	.004		0.10	
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TITLE: TO-270 WIDE BODY 16 LEAD, GULL WING					DOCUMENT NO: 98ASA10755D			REV: A	
					CASE NUMBER: 1887-01			31 AUG 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2009	• Initial Release of Data Sheet
1	Oct. 2010	• Table 1, Maximum Ratings, increased Input Power from 4.7 dBm to 20 dBm to reflect the true capability of the device, p. 2

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Freescale Semiconductor Japan Ltd.  
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Tokyo 153-0064  
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[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
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